LMT84/LMT84-Q1 1.5V, SC70/TO-92, Analog Temperature Sensors with Class-AB Output

1 Features

- LMT84-Q1 is AEC-Q100 Grade 0 qualified and is Manufactured on an Automotive Grade Flow
- Low 1.5 V Operation
- Very Accurate: ±0.4°C typical
- Wide Temperature Range of -50°C to 150°C
- Low 5.4µA Quiescent Current
- Average Sensor Gain of -5.5 mV/°C
- Packages:
  - Small SC70 (SOT 5-lead) surface mount
  - Leaded TO-92
- Output is Short-Circuit Protected
- Push-Pull Output with ±50 µA Drive Capability
- Footprint Compatible with the Industry-Standard LM20/19 and LM35 Temperature Sensors
- Cost-effective Alternative to Thermistors

2 Applications

- Automotive
- Industrial
- White Goods - Appliances
- Battery Management
- Disk Drives
- Games
- Wireless Transceivers
- Cell Phones

3 Description

The LMT84/LMT84-Q1 are precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. Its features make it suitable for many general temperature sensing applications. It can operate down to 1.5V supply with 5.4 µA power consumption making it ideal for battery powered devices. Package options including through-hole TO-92 package allows the LMT84 to be mounted on-board, off-board, to a heat sink, or on multiple unique locations in the same application. A class-AB output structure gives the LMT84/LMT84-Q1 strong output source and sink current capability that can directly drive up to 1.1 nF capacitive loads. This means it is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. It has accuracy specified in the operating range of −50°C to 150°C. The accuracy, 3-lead package options, and other features also make the LMT84/LMT84-Q1 an alternative to thermistors.

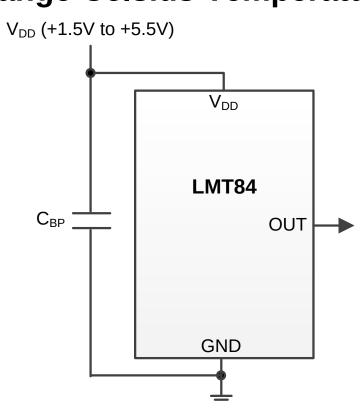
For devices with different average sensor gains and comparable accuracy the LMT85/LM85-Q1, LMT86/LMT86-Q1 and LMT87/LMT87-Q1 (For more details see Comparable Alternative Devices.)

Device Information(1)

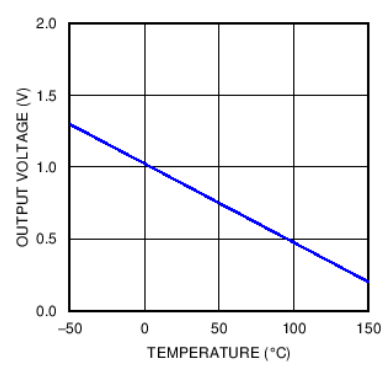
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMT84	SOT (5)	2.00 mm x 1.25 mm
	TO-92 (3)	4.3 mm x 3.5 mm
LMT84-Q1	SOT (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Full-Range Celsius Temperature Sensor (−50°C to 150°C)



Output Voltage vs Temperature



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2014) to Revision C	Page
• Deleted all mentions of TO-126 package	1
• Added TO-92 LPM pin configuration graphic	3
• Changed Handling Ratings to ESD Ratings and moved Storage Temperature to Absolute Maximum Ratings table	4
• Changed KV to V	4
• Added layout recommendation for TO-92 LP and LPM packages	15

Changes from Revision A (June 2013) to Revision B	Page
• Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, Mechanical, Packaging, and Orderable Information.	1
• Added TO-92 and TO-126 package information throughout document.	1
• Changed from 450°C/W to 275 °C/W. New specification is derived using TI ' s latest methodology.	5
• Deleted Note: The input current is leakage only and is highest at high temperature. It is typically only 0.001 µA. The 1 µA limit is solely based on a testing limitation and does not reflect the actual performance of the part.	6

Device Comparison Table[1]

ORDER NUMBER	PACKAGE	PIN	BODY SIZE (NOM)	Mounting Type
LMT84DCK	SOT (AKA[2]: SC70, DCK)	5	2.00 mm x 1.25 mm	Surface Mount
LMT84LP	TO-92 (AKA[2]: LP)	3	4.3 mm x 3.5 mm	Through-hole; straight leads
LMT84LPM	TO-92 (AKA[2]: LPM)	3	4.3 mm x 3.5 mm	Through-hole; formed leads
LMT84DCK-Q1	SOT (AKA[2]: SC70, DCK)	5	2.00 mm x 1.25 mm	Surface Mount

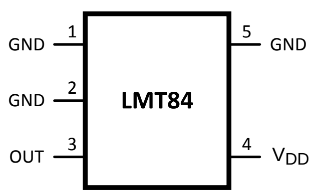
(1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.
(2) AKA = Also Known As

Comparable Alternative Devices

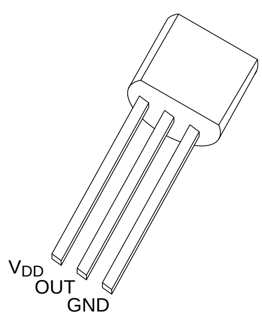
DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
LMT84/LMT84-Q1	–5.5 mV/°C	1.5V to 5.5V
LMT85/LMT85-Q1	–8.2 mV/°C	1.8V to 5.5V
LMT86/LMT86-Q1	–10.9 mV/°C	2.2V to 5.5V
LMT87/LMT87-Q1	–13.6 mV/°C	2.7V to 5.5V

6 Pin Configuration and Functions

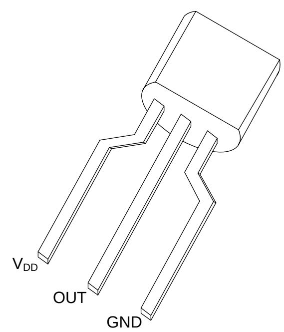
5-Pin SOT (SC70)
DCK Package
(Top View)



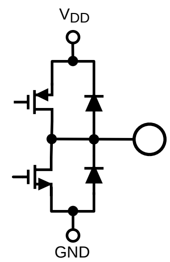
3-Pin TO-92
LP Package



3-Pin TO-92
LPM Package



Pin Functions

PIN				DESCRIPTION		
LABEL	**DCK NUMBER**	**LP NUMBER**	**LPC NUMBER**	**TYPE**	**EQUIVALENT CIRCUIT**	**FUNCTION**
GND	5			Ground		Power Supply Ground
GND	1			Ground		Power Supply Ground
OUT	3	See Pin Diagram	See Pin Diagram	Analog Output		Outputs a voltage which is inversely proportional to temperature
V_{DD}	4			Power		Positive Supply Voltage
GND	2			Ground		Power Supply Ground, (direct connection to the back side of the die)

7 Specifications

7.1 Absolute Maximum Ratings[(1)(2)]

	MIN	MAX	UNIT
Supply Voltage	−0.3	6	V
Voltage at Output Pin	−0.3	(V_{DD} + 0.5)	V
Output Current	-7	7	mA
Input Current at any pin[(3)]	-5	5	mA
Maximum Junction Temperature (T_{JMAX})		150	°C
Storage temperature T_{stg}	−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specified specific performance limits. For specifications and test conditions, see the *Electrical Characteristics*. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) *Soldering process must comply with Reflow Temperature Profile specifications. Refer to* www.ti.com/packaging.
(3) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V), the current at that pin should be limited to 5 mA.

7.2 ESD Ratings - Commercial

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins. [(1)] Applies for TO-92 package LMT84LP.	±2500	V
		Human Body Model (HBM), per JESD22-A114, all pins. Applies for SC70 package LMT84DCK.	±2500	
		Charged Device Model (CDM), per JEDEC specification JESD22-C101, all pins. [(2)] Applies for all parts.	±1000	
		Machine Model ESD stress voltage, per JEDEC specification JESD22-A115 [(3)] Applies for SC70 package LMT84DCK.	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) The machine model is 200 pF capacitor discharged directly into each pin.

7.3 ESD Ratings - Automotive

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per JESD22-A114, all pins. (1) Applies for SC70 package LMT84DCK-Q1.	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins. (2) Applies for SC70 package LMT84DCK-Q1.	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified Temperature Range:	$T_{MIN} \le T_A \le T_{MAX}$		°C
	$-50 \le T_A \le 150$		°C
Supply Voltage Range (V_{DD})	1.5	5.5	V

7.5 Thermal Information[1]

THERMAL METRIC[2]		LMT84/ LMT84-Q1	LMT84	UNIT
		DCK	LP	
		5 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [3][4]	275	167	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84	90	
$R_{\theta JB}$	Junction-to-board thermal resistance	56	146	
ψ_{JT}	Junction-to-top characterization parameter	1.2	35	
ψ_{JB}	Junction-to-board characterization parameter	55	146	

(1) For information on self-heating and thermal response time see section Mounting and Thermal Conductivity.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(3) The junction to ambient thermal resistance ($R_{\theta JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(4) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

7.6 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in Table 1.

PARAMETER	TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
Temperature Accuracy [3]	70°C to 150°C; V_{DD} = 1.5 V to 5.5 V	-2.7	±0.6	2.7	°C
	0°C to 70°C; V_{DD} = 1.5 V to 5.5 V	-2.7	±0.9	2.7	°C
	–50°C to 0°C; V_{DD} = 1.6 V to 5.5 V	-2.7	±0.9	2.7	°C
	–50°C to 150°C; V_{DD} = 2.3 V to 5.5 V		±0.4		°C

(1) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

7.7 Electrical Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = +1.5V to +5.5V. MIN and MAX limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; typical values apply for $T_A = T_J$ = 25°C.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNITS
	Sensor Gain			–5.5		mV/°C
	Load Regulation (3)	Source ≤ 50 µA, (V_{DD} - V_{OUT}) ≥ 200 mV	-1	–0.22		mV
		Sink ≤ 50 µA, V_{OUT} ≥ 200 mV		0.26	1	mV
	Line Regulation (4)			200		µV/V
I_S	Supply Current	T_A = 30°C to 150°C, (V_{DD} - V_{OUT}) ≥ 100 mV		5.4	8.1	µA
		T_A = -50°C to 150°C, (V_{DD} - V_{OUT}) ≥ 100 mV		5.4	9	µA
C_L	Output Load Capacitance			1100		pF
	Power-on Time (5)	C_L= 0 pF to 1100 pF		0.7	1.9	ms
	Output drive			±50		µA

(1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Source currents are flowing out of the LMT84/LMT84-Q1. Sink currents are flowing into the LMT84/LMT84-Q1.
(4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in Output Voltage Shift.
(5) Specified by design and characterization.

7.8 Typical Characteristics

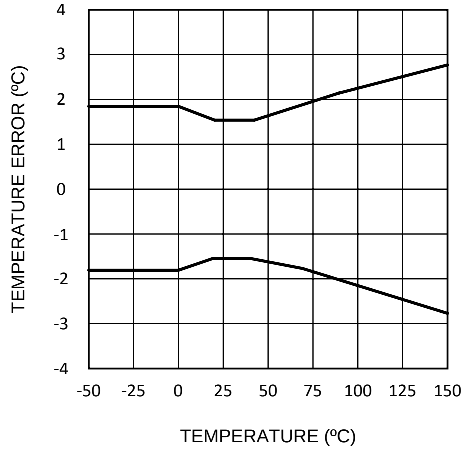


Figure 1. Temperature Error vs Temperature

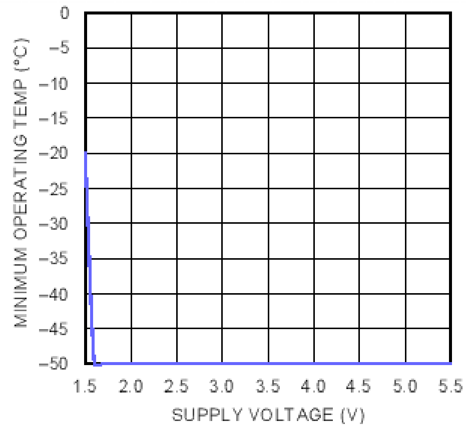


Figure 2. Minimum Operating Temperature vs Supply Voltage

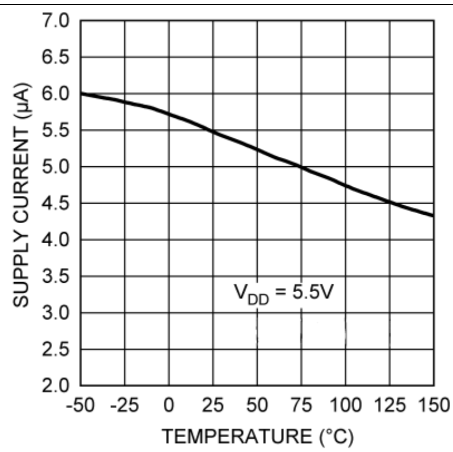


Figure 3. Supply Current vs Temperature

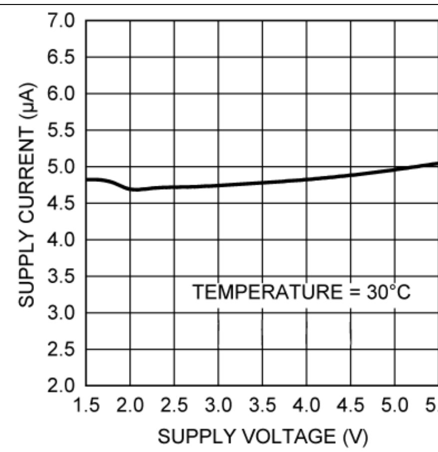


Figure 4. Supply Current vs Supply Voltage

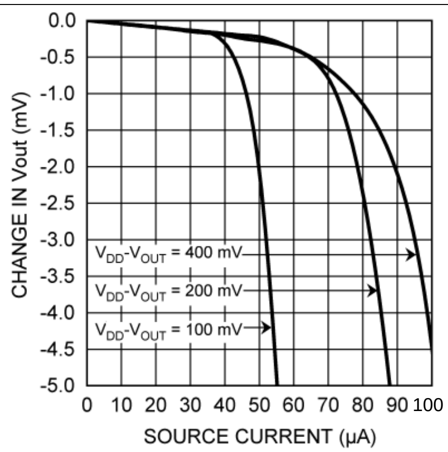


Figure 5. Load Regulation, Sourcing Current

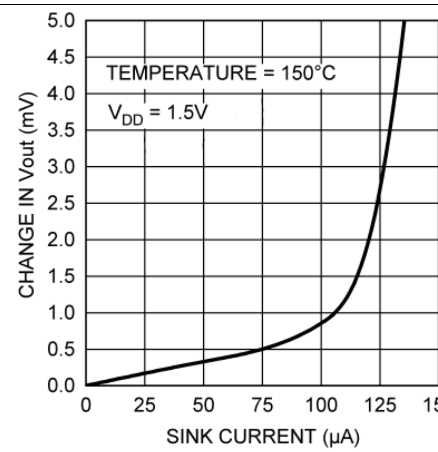


Figure 6. Load Regulation, Sinking Current

Typical Characteristics (continued)

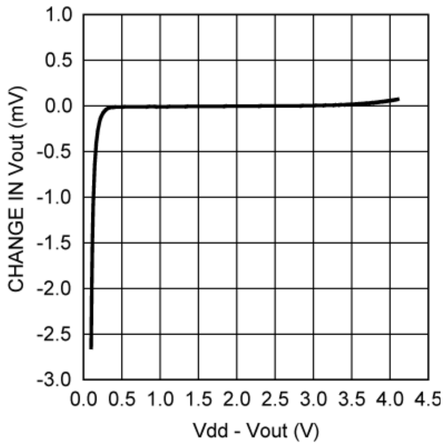


Figure 7. Change in Vout vs Overhead Voltage

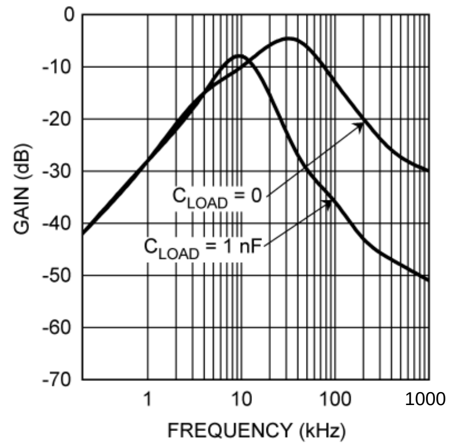


Figure 8. Supply-Noise Gain vs Frequency

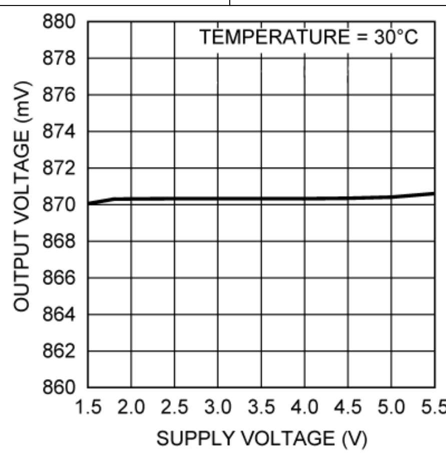


Figure 9. Output Voltage vs Supply Voltage

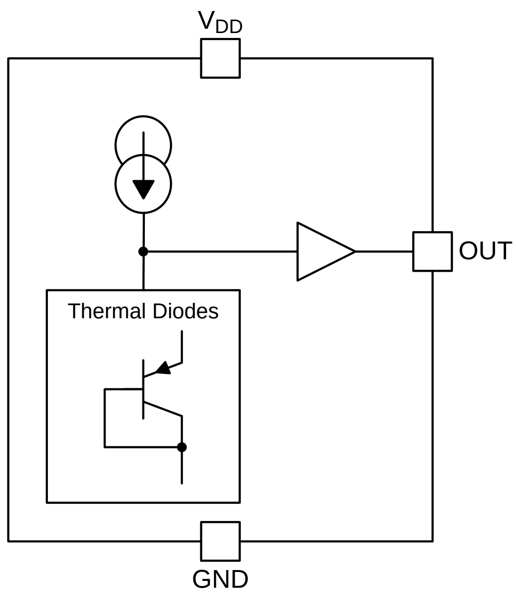
8 Detailed Description

8.1 Overview

The LMT84/LMT84-Q1 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

8.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (−50°C to 150°C)



8.3 Feature Description

8.3.1 LMT84/LMT84-Q1 Transfer Function

The output voltage of the LMT84/LMT84-Q1, across the complete operating temperature range, is shown in Table 1. This table is the reference from which the LMT84/LMT84-Q1 accuracy specifications (listed in the Accuracy Characteristics section) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the LMT84 product folder under Tools and Software Models.

Table 1. LMT84/LMT84-Q1 Transfer Table

TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)
-50	1299	-10	1088	30	871	70	647	110	419
-49	1294	-9	1082	31	865	71	642	111	413
-48	1289	-8	1077	32	860	72	636	112	407
-47	1284	-7	1072	33	854	73	630	113	401
-46	1278	-6	1066	34	849	74	625	114	396
-45	1273	-5	1061	35	843	75	619	115	390
-44	1268	-4	1055	36	838	76	613	116	384
-43	1263	-3	1050	37	832	77	608	117	378
-42	1257	-2	1044	38	827	78	602	118	372
-41	1252	-1	1039	39	821	79	596	119	367
-40	1247	0	1034	40	816	80	591	120	361

Feature Description (continued)

Table 1. LMT84/LMT84-Q1 Transfer Table (continued)

TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)
-39	1242	1	1028	41	810	81	585	121	355
-38	1236	2	1023	42	804	82	579	122	349
-37	1231	3	1017	43	799	83	574	123	343
-36	1226	4	1012	44	793	84	568	124	337
-35	1221	5	1007	45	788	85	562	125	332
-34	1215	6	1001	46	782	86	557	126	326
-33	1210	7	996	47	777	87	551	127	320
-32	1205	8	990	48	771	88	545	128	314
-31	1200	9	985	49	766	89	539	129	308
-30	1194	10	980	50	760	90	534	130	302
-29	1189	11	974	51	754	91	528	131	296
-28	1184	12	969	52	749	92	522	132	291
-27	1178	13	963	53	743	93	517	133	285
-26	1173	14	958	54	738	94	511	134	279
-25	1168	15	952	55	732	95	505	135	273
-24	1162	16	947	56	726	96	499	136	267
-23	1157	17	941	57	721	97	494	137	261
-22	1152	18	936	58	715	98	488	138	255
-21	1146	19	931	59	710	99	482	139	249
-20	1141	20	925	60	704	100	476	140	243
-19	1136	21	920	61	698	101	471	141	237
-18	1130	22	914	62	693	102	465	142	231
-17	1125	23	909	63	687	103	459	143	225
-16	1120	24	903	64	681	104	453	144	219
-15	1114	25	898	65	676	105	448	145	213
-14	1109	26	892	66	670	106	442	146	207
-13	1104	27	887	67	664	107	436	147	201
-12	1098	28	882	68	659	108	430	148	195
-11	1093	29	876	69	653	109	425	149	189
								150	183

Although the LMT84/LMT84-Q1 is very linear, its response does have a slight umbrella parabolic shape. This shape is very accurately reflected in Table 1. The Transfer Table can be calculated by using the parabolic equation.

$$V_{TEMP}(mV) = 870.6mV - \left[5.506\frac{mV}{°C}(T - 30°C)\right] - \left[0.00176\frac{mV}{°C^2}(T - 30°C)^2\right] \tag{1}$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. Equation 1 can be solved for T resulting in:

$$T = \frac{5.506 - \sqrt{(-5.506)^2 + 4 \times 0.00176 \times (870.6 - V_{TEMP}(mV))}}{2 \times (-0.00176)} + 30 \tag{2}$$

For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range from the Table using the two-point equation:

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1}\right) \times (T - T_1) \tag{3}$$

Where V is in mV, T is in °C, T_1 and V_1 are the coordinates of the lowest temperature, T_2 and V_2 are the coordinates of the highest temperature.

For example, if we want to resolve this equation, over a temperature range of 20°C to 50°C, we would proceed as follows:

$$V - 925\text{ mV} = \left(\frac{760\text{ mV} - 925\text{ mV}}{50^{o}\text{C} - 20^{o}\text{C}}\right) \times (T - 20^{o}\text{C}) \quad (4)$$

$$V - 925\text{ mV} = (-5.50\text{ mV} / ^{o}\text{C}) \times (T - 20^{o}\text{C}) \quad (5)$$

$$V = (-5.50\text{ mV} / ^{o}\text{C}) \times T + 1035\text{ mV} \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

8.4 Device Functional Modes

8.4.1 Mounting and Thermal Conductivity

The LMT84/LMT84-Q1 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT84/LMT84-Q1 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT84/LMT84-Q1 will also affect the temperature reading.

Alternatively, the LMT84/LMT84-Q1 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT84/LMT84-Q1 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or V_{DD}, the output from the LMT84/LMT84-Q1 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ($R_{\theta JA}$ or θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. The equation used to calculate the rise in the LMT84/LMT84-Q1's die temperature is:

$$T_J = T_A + \theta_{JA}\left[(V_{DD}I_S) + (V_{DD} - V_O)\, I_L\right] \quad (7)$$

where T_A is the ambient temperature, I_S is the supply current, I_L is the load current on the output, and V_O is the output voltage. For example, in an application where T_A = 30°C, V_{DD} = 5 V, I_S = 5.4 µA, V_{OUT} = 871 mV, and I_L = 2 µA, the junction temperature would be 30.015°C, showing a self-heating error of only 0.015°C. Since the LMT84/LMT84-Q1's junction temperature is the actual temperature being measured, care should be taken to minimize the load current that the LMT84/LMT84-Q1 is required to drive. Thermal Information(1) shows the thermal resistance of the LMT84/LMT84-Q1.

8.4.2 Output Noise Considerations

A push-pull output gives the LMT84/LMT84-Q1 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT84/LMT84-Q1 is ideal for this and other applications which require strong source or sink current.

The LMT84/LMT84-Q1 supply-noise gain (the ratio of the AC signal on V_{OUT} to the AC signal on V_{DD}) was measured during bench tests. Its typical attenuation is shown in Figure 8 found in the Typical Characteristics section. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT84/LMT84-Q1.

8.4.3 Capacitive Loads

The LMT84/LMT84-Q1 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the LMT84/LMT84-Q1 can drive a capacitive load less than or equal to 1100 pF as shown in Figure 10. For capacitive loads greater than 1100 pF, a series resistor may be required on the output, as shown in Figure 11.

(1) For information on self-heating and thermal response time see section Mounting and Thermal Conductivity.

Device Functional Modes (continued)

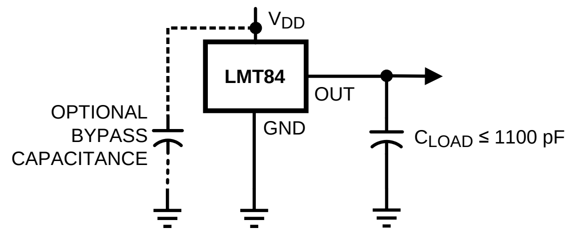


Figure 10. LMT84 No Decoupling Required for Capacitive Loads Less than 1100 pF

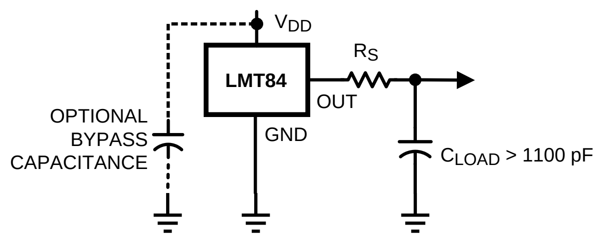


Figure 11. LMT84 with Series Resistor for Capacitive Loading Greater than 1100 pF

C_{LOAD}	Minimum R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	800 Ω

8.4.4 Output Voltage Shift

The LMT84/LMT84-Q1 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT}. The shift typically occurs when V_{DD}- V_{OUT} = 1.0V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT}. Since the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic. The accuracy specifications in the Accuracy Characteristics table already include this possible shift.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Applications Information

The LMT84/LMT84-Q1 features make it suitable for many general temperature sensing applications. It can operate down to 1.5V supply with 5.4 uA power consumption making it ideal for battery powered devices. Package options including through-hole TO-92 package allows the LMT84 to be mounted on-board, off-board, to a heat sink, or on multiple unique locations in the same application.

9.2 Typical Applications

9.2.1 Connection to an ADC

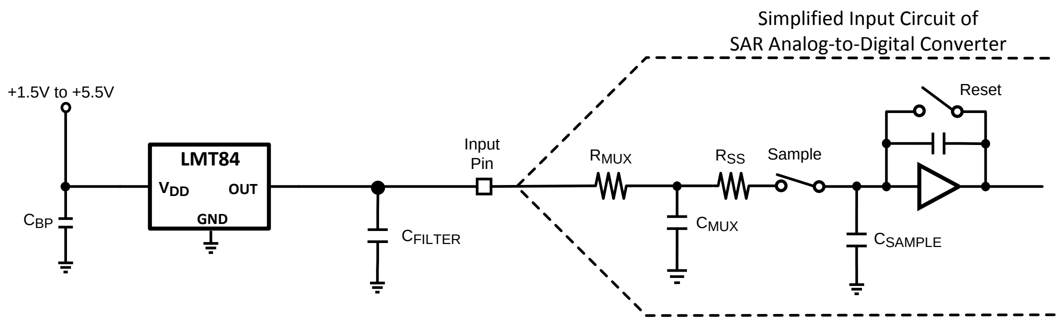


Figure 12. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

9.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT84/LMT84-Q1 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}).

9.2.1.2 Detailed Design Procedure

The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Since not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

9.2.1.3 Application Curves

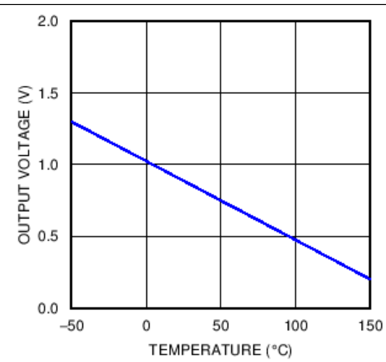


Figure 13. Analog Output Transfer Function

9.2.2 Conserving Power Dissipation with Shutdown

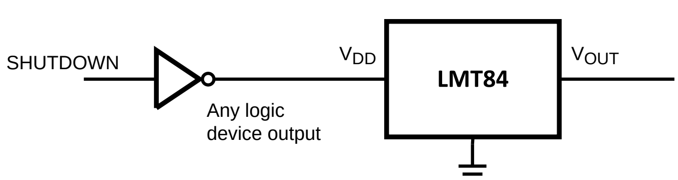


Figure 14. Simple Shutdown Connection of the LMT84

Typical Applications (continued)

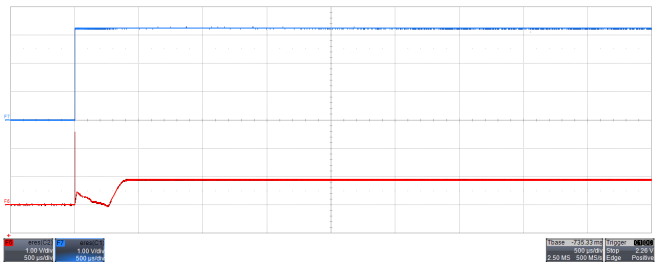
9.2.2.1 Design Requirements

Since the power consumption of the LMT84 is less than 9 µA it can simply be powered directly from any logic gate output, thus not requiring a specific shutdown pin. The device can even be powered directly from a micro controller GPIO. In this way it can easily be turned off for cases such as battery powered systems where power savings is critical.

9.2.2.2 Detailed Design Procedure

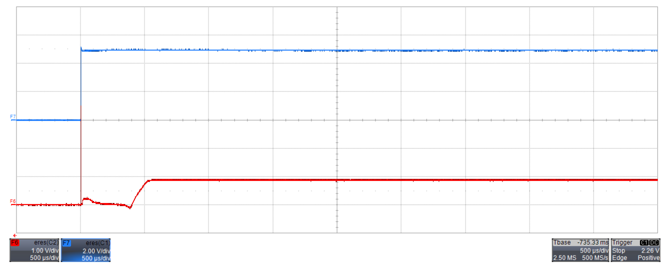
Simply connect the V_{DD} pin of the LMT84 directly to the logic shutdown signal from a microcontroller.

9.2.2.3 Application Curves



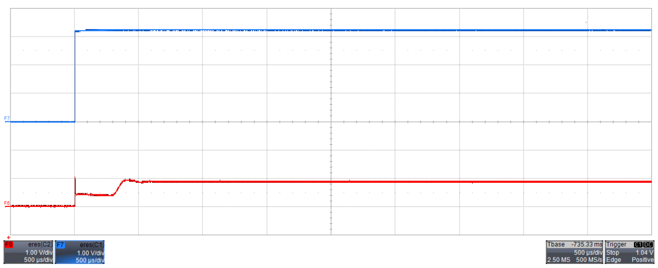
Time: 500 µsec/div; Top trace: V_{DD} 1 V/div;
Bottom trace: OUT 1 V/div

Figure 15. Output Turn-on Response Time Without a Capacitive Load and V_{DD}= 3.3V



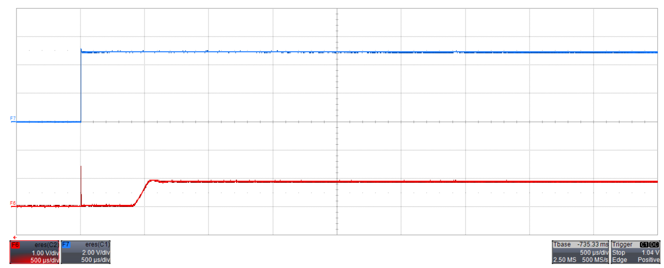
Time: 500 µsec/div; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 16. Output Turn-on Response Time Without a Capacitive Load and V_{DD}= 5V



Time: 500 µsec/div; Top trace: V_{DD} 1 V/div;
Bottom trace: OUT 1 V/div

Figure 17. Output Turn-on Response Time With 1.1 Nf Capacitive Load and V_{DD}= 3.3V



Time: 500 µsec/div; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 18. Output Turn-on Response Time With 1.1 Nf Capacitive Load and V_{DD}= 5V

10 Power Supply Recommendations

The LMT84's low supply current and supply range of 1.5V to 5.5V allow the device to easily be powered from many sources.

Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems it may be necessary to add bypass capacitors to lower the noise that is coupled to the LMT84's output.

11 Layout

11.1 Layout Guidelines

The LMT84 is extremely simple to layout. If a power supply bypass capacitor is used is should be connected as shown in the Layout Example.

11.2 Layout Example

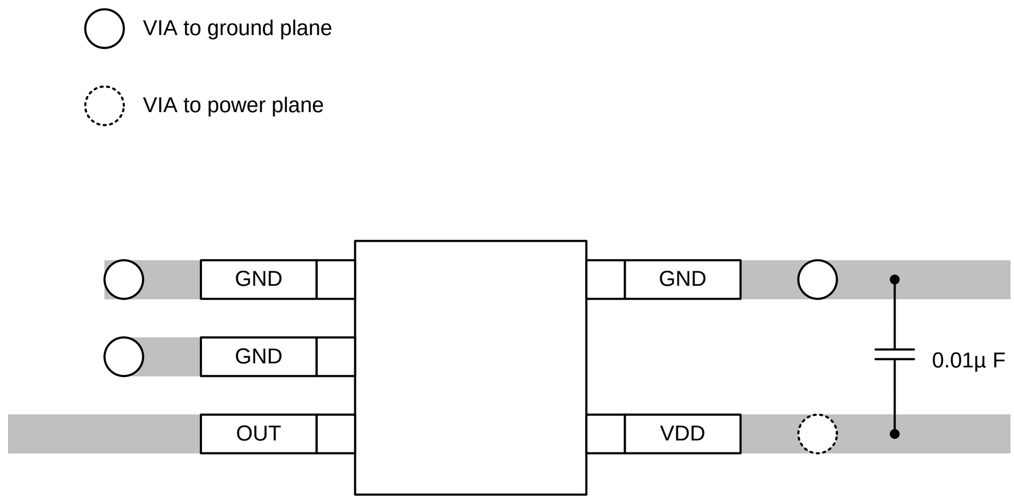


Figure 19. SC70 Package Recommended Layout

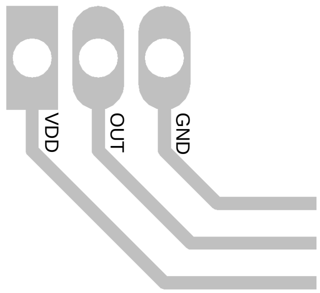


Figure 20. TO-92 LP Package Recommended Layout

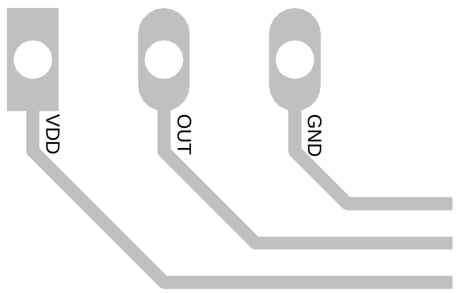


Figure 21. TO-92 LPM Package Recommended Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMT84	Click here	Click here	Click here	Click here	Click here
LMT84-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMT84DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	BNA	Samples
LMT84DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	BNA	Samples
LMT84LP	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-50 to 150	LMT84	Samples
LMT84LPM	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-50 to 150	LMT84	Samples
LMT84QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	BOA	Samples
LMT84QDCKTQ1	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	BOA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMT84, LMT84-Q1 :

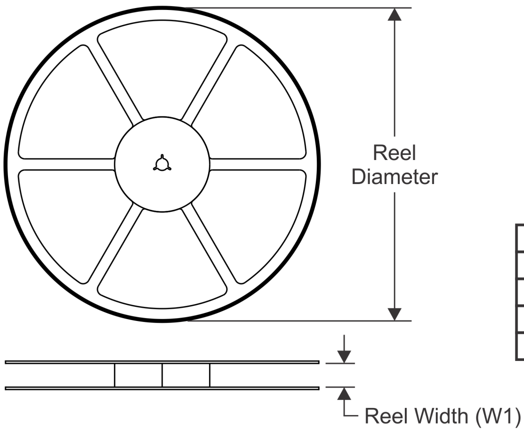
- Catalog: LMT84
- Automotive: LMT84-Q1

NOTE: Qualified Version Definitions:

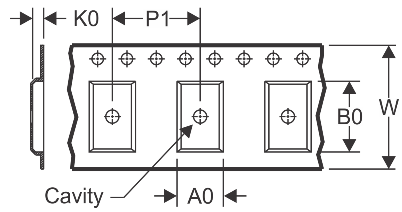
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

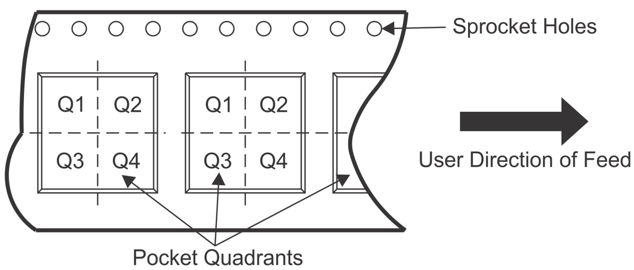


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

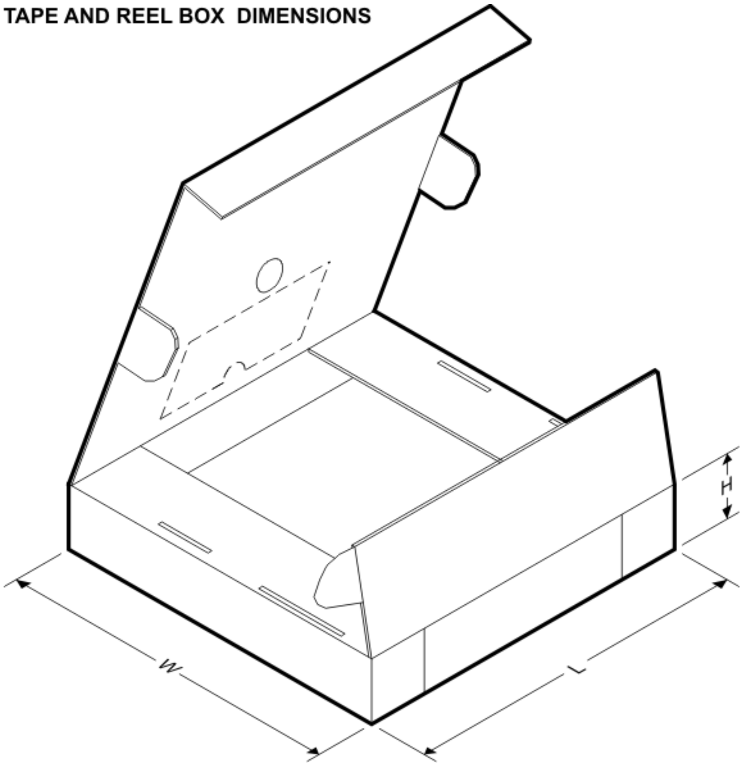
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT84DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMT84DCKT	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMT84QDCKRQ1	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMT84QDCKTQ1	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT84DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
LMT84DCKT	SC70	DCK	5	250	210.0	185.0	35.0
LMT84QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
LMT84QDCKTQ1	SC70	DCK	5	250	210.0	185.0	35.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

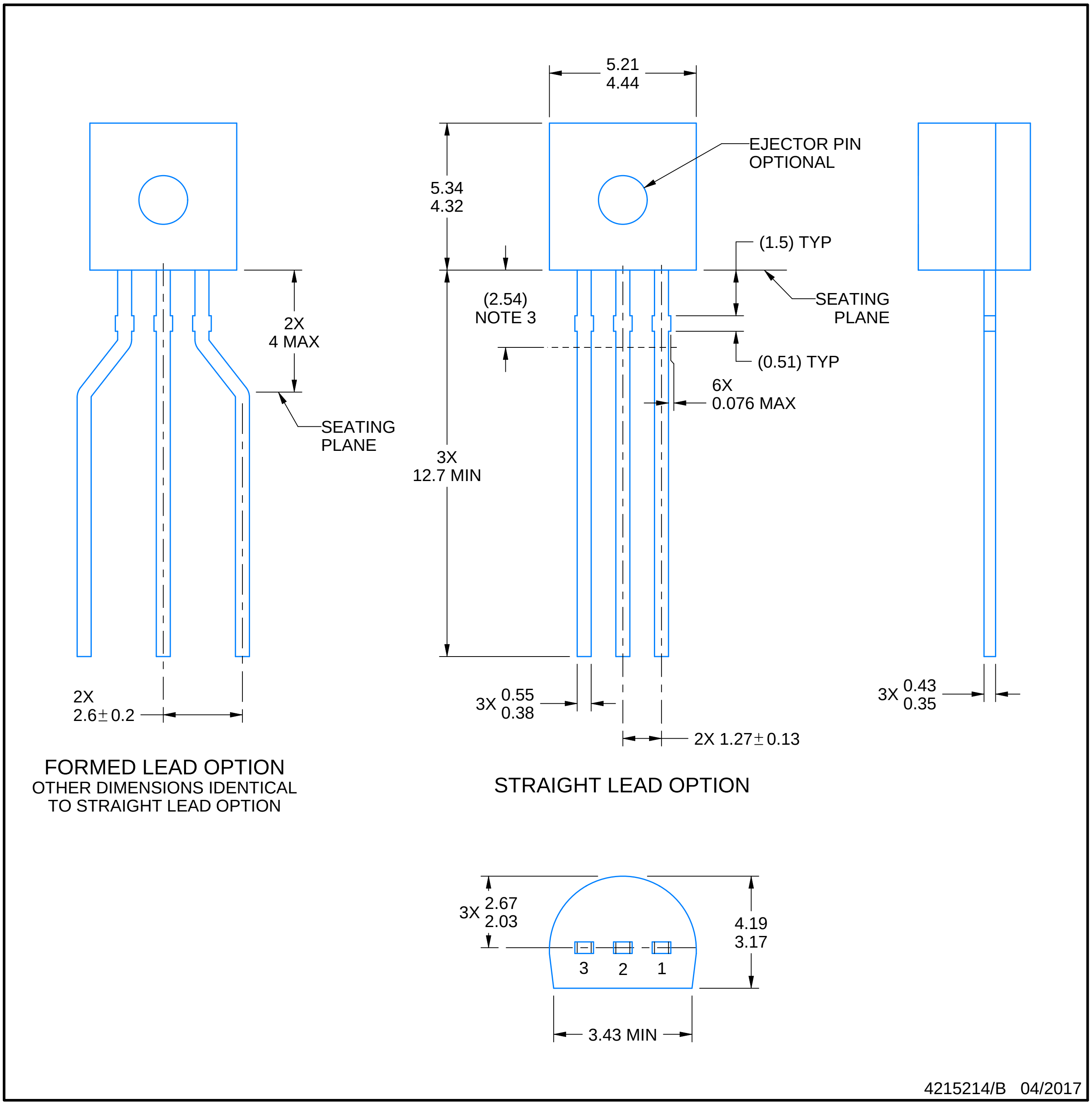
4040001-2/F

PACKAGE OUTLINE

LP0003A

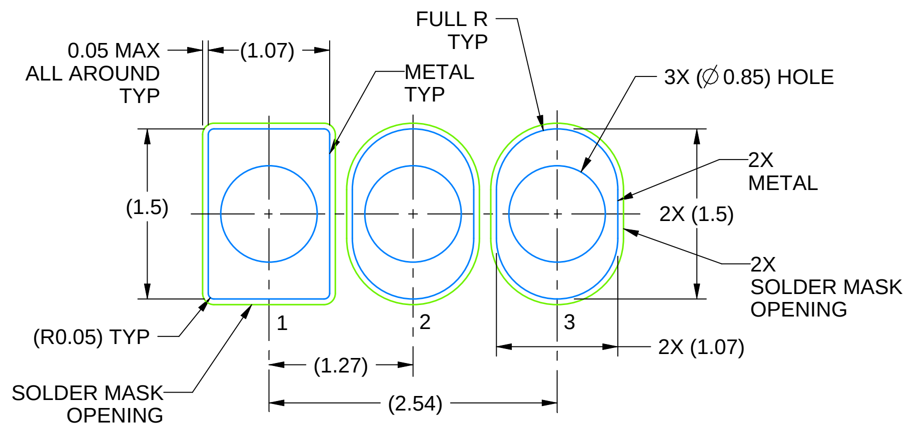
TO-92 - 5.34 mm max height

TO-92

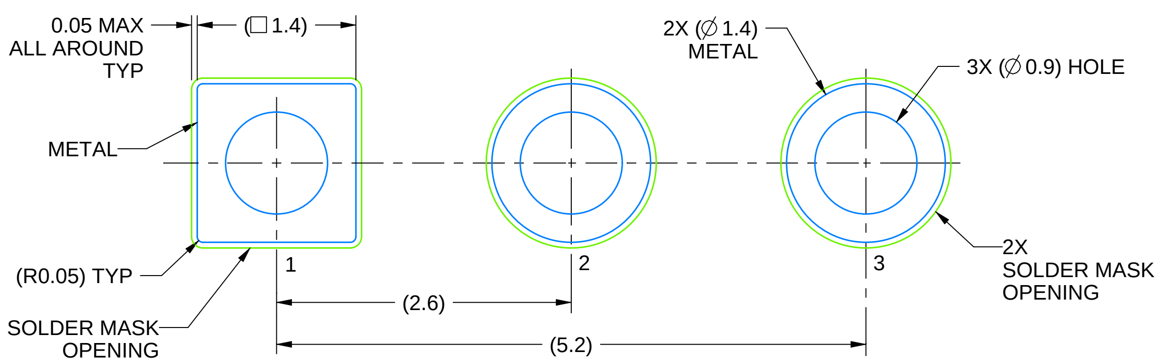


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

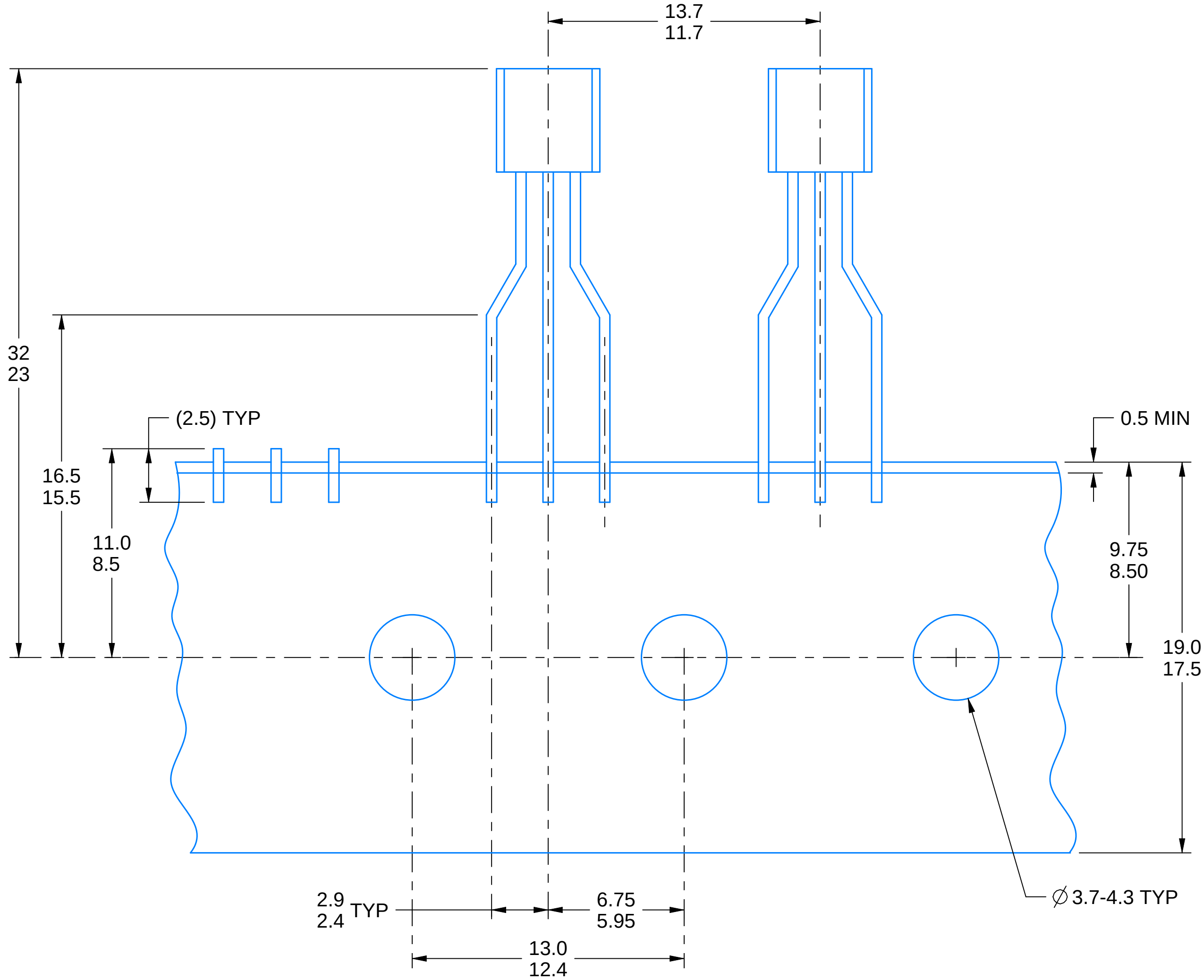


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

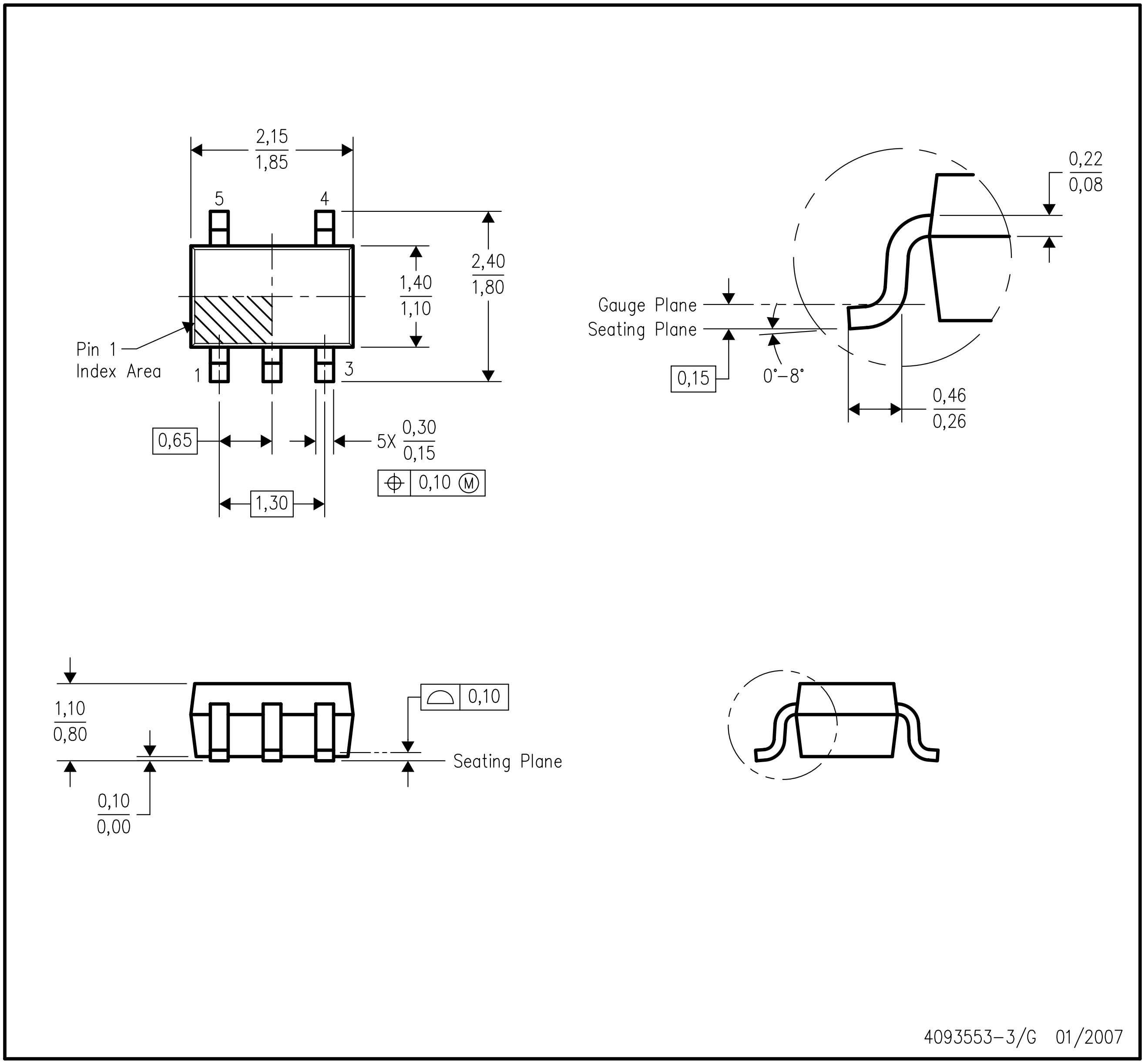
4215214/B 04/2017



FOR FORMED LEAD OPTION PACKAGE

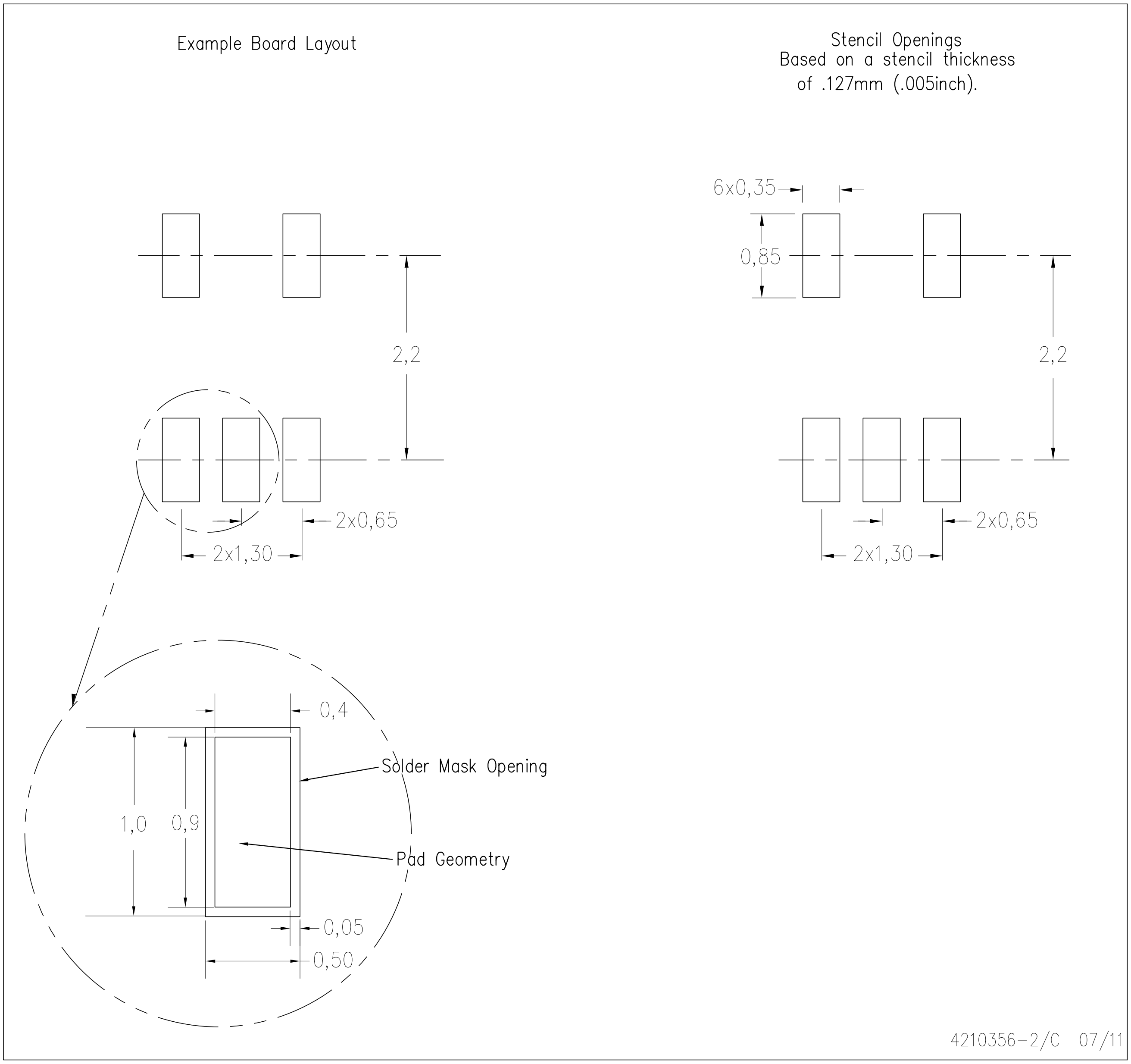
4215214/B 04/2017

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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